The VERITAS Array Trigger

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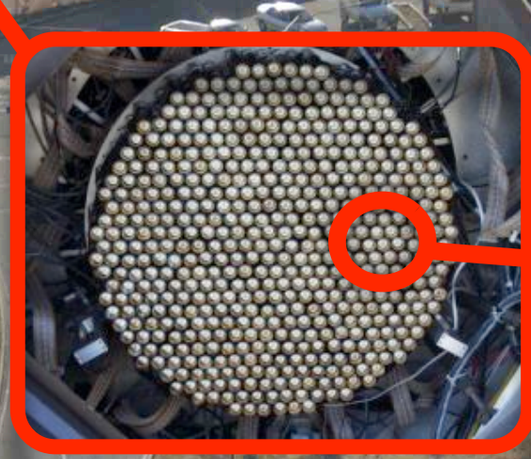
VERITAS 3 Level Trigger

4 x 12m Davies-Cotton Reflectors

499 Pixel Cameras



Photonis XP PMT

VERITAS 3 Level Trigger

Trigger can be thought of as:

L1: Pixel Level

L2: Camera Level

L3: Array Level

L1

Preamplifiers (6.66x gain)

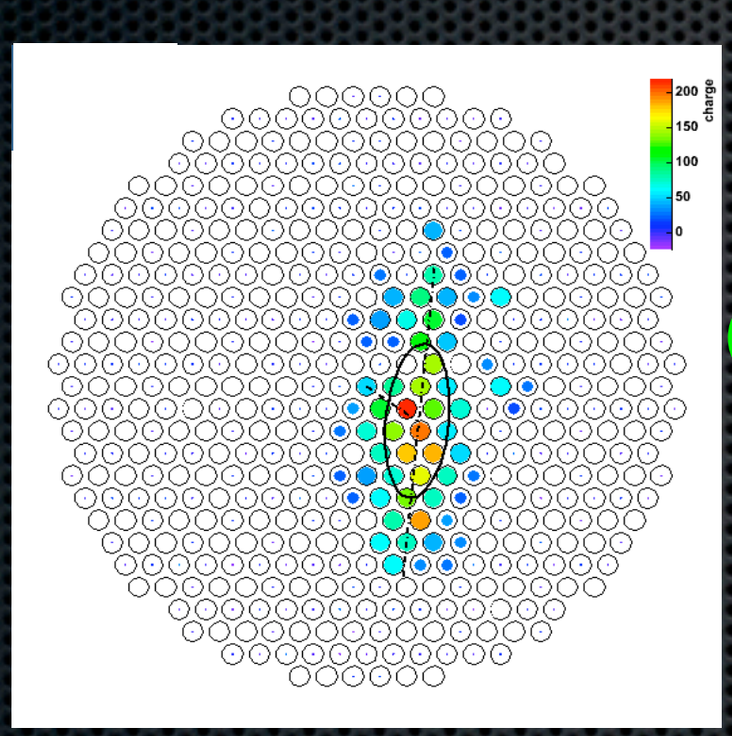
500 Msps
FADCs
(65 μs Ring Memory Buffer)

CFD: L1 Trigger is cast if voltage exceeds programmable threshold (50 mV)

L2

L1 Triggers (~MHz)

Signal Splitter Crate
(19 Cards: 59 overlapping pixel patches each)



Custom Built Pattern Selection Trigger
Looks for combinations of 3 adjacent pixels.

L3

L2 Triggers From All Tels
(1-2 kHz)

(via DAT module communication)

Central Trailer L3 Decision:
Cast Trigger if 2/4 Tels show L2 trigger w/in programmable time window (100 ns)

Triggers (~200 Hz) sent back to each Tel

Each Tels' FADC buffer read out

Overall:

L1: CFD Trigger

~MHz

PMTs

L2: Camera Pattern Trigger

FADCs

200-300 Hz

~1-2 kHz

L3: Array Level Trigger

All Tel's L2s

Event Builder

When L3 Trigger is cast....

- During the FADC readout time, system can not process triggers->10% dead-time for array trigger @ 200-300 Hz (leaves room for improvement)
- Most of these triggers are cosmic rays/NSB: discarded during offline analysis (parallax comparison is one discrimination parameter)

A Topological Pattern Trigger-

- By implementing a CR rejection technique (parallax comparison) online in the trigger decision, efficiency for detecting real gammas greatly improves efficiency, sensitivity, threshold, morale.....
- PAT spies information from L1 CFD trigger level- does not effect normal operation during testing